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AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A method of assigning thread priority comprising:

assigning priority to a first thread in a multi threaded processor;

loading a preliminary value to a thread precedence counter;

assigning priority to a second thread in response to expiration of said thread precedence counter;

determining if there is an indication of approaching instruction side starvation for said first thread wherein instruction fetching for said first thread would be blocked due to processing one or more instructions from another thread; and

incrementing a value stored in said first starting counter in response to an indication of approaching instruction side starvation for said first thread.

2. (Original) The method of claim 1 wherein said preliminary value is based on a value stored in a first starting counter associated with said first thread.

3. (Cancelled)

4. (Previously Presented) The method of claim 2 wherein determining if there is an indication of approaching instruction side starvation for said first thread includes

determining if each of a plurality of conditions are true, the plurality of conditions including each of the following

if the processor is operating in a multithreaded processing mode;

if the first thread has no instructions in an execution pipeline of said processor; and

if the first thread is attempting to fetch instructions from a memory.

5. (Currently Amended) The method of claim 4 wherein ~~when incrementing~~ if the value stored in the first starting counter is incremented, said value is incremented geometrically.

6. (Original) The method of claim 5 wherein said value is incremented geometrically by left-shifting a binary 1 bit into said value.

7. (Currently Amended) A method of assigning thread priority comprising:

assigning priority to a first thread in a multi threaded processor; and

assigning priority to a second thread in response to one of a plurality of conditions being true, the conditions consisting of

if a thread precedence counter expires;

if processing of said first thread retires an instruction from said first thread; and

if there is not an indication of approaching instruction side starvation for said first thread wherein instruction fetching for said first thread would be blocked due to processing one or more instructions from another thread.

8. (Previously Presented) The method of claim 7 wherein said indication of approaching instruction side starvation for said first thread includes each of a plurality of conditions being true, the plurality of conditions including each of the following

if the processor is operating in a multithreaded processing mode;

if the first thread has no instructions in an execution pipeline of said processor; and

if the first thread is attempting to fetch instructions from a memory.

9. (Currently Amended) A processor, comprising:

control logic to assign priority to one of at least first and second threads; and

a thread precedence counter coupled to said control logic wherein priority is assigned to said second thread after said thread precedence counter expires wherein said control logic is to determine if there is an indication of approaching instruction side starvation for said first thread wherein instruction fetching for said first thread would be blocked due to processing one or more instructions from another thread, and to increment a value stored in said first starting counter if there is an indication of approaching instruction side starvation for said first thread.

10. (Original) The processor of claim 9 wherein a preliminary value for said thread precedence counter is based on a value stored in a first starting counter associated with said first thread.

11. (Cancelled)

12. (Currently Amended) The processor of [~~claim 11~~] claim 9 wherein said control logic is to determine if there is an indication of approaching instruction side starvation for said first thread by determining if each of a plurality of conditions are true, the plurality of conditions including each of the following

if the processor is operating in a multithreaded processing mode;

if the first thread has no instructions in an execution pipeline of said processor; and

if the first thread is attempting to fetch instructions from a memory.

13. (Original) The processor of claim 12 wherein said control logic is to increment the value stored in the first starting counter geometrically.

14. (Original) The processor of claim 13 wherein said value is to be incremented geometrically by left-shifting a binary 1 bit into said value.

15. (Currently Amended) A processor comprising:

control logic to assign priority to a first thread and to assign priority to a second thread in response to one of a plurality of conditions being true, the conditions consisting of

if a processing counter expires;

if processing of said first thread retires an instruction from said first thread; and

if there is not an indication of approaching instruction side starvation for said first thread wherein instruction fetching for said first thread would be blocked due to processing one or more instructions from another thread.

16. (Previously Presented) The processor of claim 15 wherein said indication of approaching instruction side starvation for said first thread includes each of a plurality of conditions being true, the plurality of conditions including each of the following

if the processor is operating in a multithreaded processing mode;

if the first thread has no instructions in an execution pipeline of said processor; and

if the first thread is attempting to fetch instructions from a memory.

17. (Currently Amended) A computer system comprising:

a memory to store instructions for first and second threads;

a processor including

control logic coupled to said memory to assign priority between said first and second threads; and

a thread precedence counter coupled to said control logic wherein priority is assigned to said second thread after said thread precedence counter expires wherein said control logic is to determine if there is an indication of approaching instruction side starvation for said first thread wherein instruction fetching for said first thread would be blocked due to processing one or more instructions from another thread and to increment a value stored in said first starting counter in response to an indication of approaching instruction side starvation for said first thread.

18. (Original) The computer system of claim 17 wherein a preliminary value for said thread precedence counter is based on a value stored in a first starting counter associated with said first thread.

19. (Cancelled)

20. (Previously Presented) The computer system of claim 18 wherein said control logic is determine if there is an indication of approaching instruction side starvation for said first thread by determining if each of a plurality of conditions are true, the plurality of conditions including each of the following

if the processor is operating in a multithreaded processing mode;

if the first thread has no instructions in an execution pipeline of said processor;

and

if the first thread is attempting to fetch instructions from a memory.

21. (Original) The computer system of claim 20 wherein said control logic is to increment the value stored in the first starting counter geometrically.

22. (Original) The computer system of claim 21 wherein said value is to be incremented geometrically by left-shifting a binary 1 bit into said value.

23. (Currently Amended) A computer system comprising:

a memory to store instructions for first and second threads;

a processor including

control logic to assign priority to said first thread and to assign priority to said second thread in response to one of a plurality of conditions being true, the conditions consisting of:

if a thread precedence counter expires;

if processing of said first thread retires an instruction from said first thread; and

if there is not an indication of approaching instruction side starvation for said first thread <u>wherein instruction fetching for said first thread would be blocked due to processing one or more instructions from another thread</u>.

24. (Previously Presented) The computer system of claim 23 wherein said indication of approaching instruction side starvation for said first thread includes each of a plurality of conditions being true, the plurality of conditions including each of the following

if the processor is operating in a multithreaded processing mode;

if the first thread has no instructions in an execution pipeline of said processor; and

if the first thread is attempting to fetch instructions from a memory.

25. (Currently Amended) A set of instructions residing in a storage medium, said set of instructions to be executed by a processor to handle processing of at least first and second threads in parallel and assign thread priority comprising:

assigning priority to said first thread;

loading a preliminary value to a thread precedence counter;

assigning priority to said second thread after said thread precedence counter expires determining if there is an indication of approaching instruction side starvation for said first thread wherein instruction fetching for said first thread would be blocked due to processing one or more instructions from another thread; and

incrementing a value stored in said first starting counter is incremented in response to an indication of approaching instruction side starvation for said first thread.

26. (Original) The set of instructions of claim 25 wherein said preliminary value is based on a value stored in a first starting counter associated with said first thread.

27. (Cancelled)

28. (Previously Presented) The set of instructions of claim 26 wherein determining if there is an indication of approaching instruction side starvation for said first thread includes determining if each of a plurality of conditions are true, the plurality of conditions including each of the following

if the processor is operating in a multithreaded processing mode;

if the first thread has no instructions in an execution pipeline of said processor; and

if the first thread is attempting to fetch instructions from a memory.

29. (Currently Amended) The set of instructions of claim 28 wherein ~~when incrementing~~ if the value stored in the first starting counter is incremented, said value is incremented geometrically.

30. (Original) The set of instructions of claim 29 wherein said value is incremented geometrically by left-shifting a binary 1 bit into said value.